# Cubic AlGaN/GaN Hetero-Junction Field-Effect Transistors with Normally-on and Normally-off Characteristics

E. Tschumak

*University of Paderborn, Faculty of Science, Department of Physics, Warburger Straße 100*
*D-33098 Paderborn, Germany*

**Abstract.** The growth of cubic group III-nitrides is a direct way to eliminate polarization effects, which inherently limit the fabrication of normally-off hetero-junction field-effect transistors (HFETs) in GaN technology. HFET structures were fabricated of non-polar cubic AlGaN/GaN hetero layers grown by plasma assisted molecular beam epitaxy on free standing 3C-SiC (001). The electrical insulation of 3C-SiC was realized by $Ar^+$ implantation before c-AlGaN/GaN growth. HFETs with normally-off and normally-on characteristics were fabricated of cubic AlGaN/GaN. Capacitance-voltage characteristics of the gate contact were performed to detect the electron channel at the c-AlGaN/GaN hetero-interface.

**Keywords:** non-polar cubic GaN, AlGaN, HFET, field effect.
**PACS:** 81.15.Hi, 72.20.-i, 73.50.-h, 85.30.TV

## INTRODUCTION

AlGaN/GaN hetero-junction field-effect transistors (HFETs) are presently of major interest for use in electronic devices, in particular for high-power and high-frequency amplifiers. This is motivated by their potential in commercial and military applications, e. g. in communication systems, radar, wireless stations, high-temperature electronics and high-power solid-state switching. Currently, state of the art HFETs are fabricated of the *c*-plane surface of wurzite (hexagonal) AlGaN/GaN hetero-structures. Their inherent spontaneous and piezoelectric polarization fields produce extraordinary large sheet carrier concentrations at the AlGaN/GaN hetero-interface. Therefore, conventional AlGaN/GaN HFETs are of the normally-on type (depletion mode) with threshold voltage ($V_{th}$) typically between -10 V and -4 V [1]-[3].

However, for switching devices and digital electronics field-effect transistors (FET) with normally-off (enhancement mode) characteristics are desirable. Therefore, several researcher groups strive for realization of GaN based enhancement mode devices using diverse techniques. HFETs of *c*-plane AlGaN/GaN with normally-off operations have been fabricated by growing a thinner AlGaN barrier layer with low Al mole fraction [4], implanting fluorine into the barrier under the gate [5], recessed gate structure [6] and growing a thin InGaN cap layer [7], [8]. Some groups used non-polar *a*-plane AlGaN/GaN to fabricate HFETs [9], [10] and demonstrated that the electrical output characteristics of these devices are different for different gate finger orientations on *a*-plane layers. However, no field-effect transistors have been realized with non-polar cubic group III-nitrides to date, although it was discussed recently by Abe et al. [11] that they would offer to fabricate HFETs without undesirable parasitic piezoelectric and spontaneous polarization fields and with equal electrical properties for all gate orientations. Furthermore, the cubic nitrides would allow using the same technology for normally-on and normally-off devices.

In this paper we summarize results of cubic AlGaN/GaN (c-AlGaN/GaN) hetero-junction field-effect transistors (HFETs) and introduce their output and transfer characteristics with both normally-on and normally-off behavior.



Downloaded 22 Dec 2010 to 158.12.36.78. Redistribution subject to AIP license or copyright; see http://proceedings.aip.org/about/rights_permissions

## EXPERIMENTS

Cubic AlGaN/GaN hetero-structures for HFETs were grown by plasma-assisted molecular beam epitaxy (MBE). In order to minimize hexagonal inclusions in our layers and to obtain optimum interface roughness a coverage of one monolayer Ga was established during growth [12]. The substrate growth temperature was 720 °C. The growth rate of the samples was 115-120 nm/h. As substrates we used free standing 3C-SiC (001). The surface of the substrates was treated by $Ar^+$ implantation to form a damage layer near the surface. In a previous study we showed that this damage acts as insulation layer [13].

Two different cubic AlGaN/GaN hetero structures (HFET A and HFET B) with similar crystalline properties were investigated. The surface morphology of the samples was characterized by atomic force microscopy (AFM). The quality of the hetero-structures and the Al content in the c-AlGaN top layer was analyzed using high-resolution X-ray diffraction (HRXRD).

For the source and drain of the devices 10 nm of the c-AlGaN top layer were removed by reactive ion etching (RIE) with $SiCl_4$ following by thermal evaporation of Ti/Al/Ni/Au (15 nm/50 nm/15 nm/50 nm) and annealing at 850 °C for 30 s in nitrogen atmosphere to form contacts with ohmic characteristics. Then c-AlGaN/GaN mesas were formed by $SiCl_4$ RIE in order to separate single devices. Gate fingers were fabricated by evaporation of Pd/Ni/Au (15 nm/15 nm/50 nm) and subsequent annealing at 400 °C for 10 min. This procedure decreased the reverse current density of our contacts more than one order of magnitude. This is in good agreement with earlier findings where it was found that annealing of metal contacts on c-III-nitrides reduces the leakage current significantly [14], [15]. Our devices have a gate length of 2 µm, a gate width of 25 µm and a source-to-drain spacing of 8 µm. Finally, contact pads were thermally evaporated onto a 250 nm thick $SiO_2$ layer which was deposited around the FET devices for isolation.

## HFET with Normally-on Characteristics

HFET A with normally-on characteristics consists of a 60 nm unintentional doped (UID) c-GaN nucleation layer followed by 580 nm carbon doped c-GaN:C used to minimize the shunt current through the c-GaN buffer layer [13]. For carbon doping a self-made $CBr_4$ source was used. A 34 nm thick homogeneously silicon doped c-$Al_{0.36}Ga_{0.64}N$:Si cap layer with carrier concentration of $n=1.5\times10^{18}$ cm$^{-3}$ was grown on top of the sample. The full width at half maximum (FWHM) of the cubic GaN (002) rocking curve was 25 arcmin. The root-mean square (RMS) roughness of the c-$Al_{0.36}Ga_{0.64}N$/GaN surface measured in a 5×5 µm$^2$ scan was 5 nm.

Due to the silicon doping of the c-AlGaN:Si barrier layer gate contact deposited directly on samples surface offers high reverse conductivity. Thus, for the HFET A the sample was thermally annealed at 600 °C in air for 10 min to form a thin oxide film on AlGaN:Si surface for decreasing of the gate conductivity. This process step was introduced after the source/drain contact metallization previous to the gate contact metallization. Our investigations showed that the resistance of ohmic contacts is increased by more than one order of magnitude by this annealing process. Thus, the output characteristics of the device are significantly limited by source and drain contact resistance.

The room temperature output characteristics of HFET A are depicted in Figure 1 (a). The gate voltage was varied between $V_G$=-10 V and $V_G$ =4 V. Apart from the shunt current (red curve) caused by gate leakage in reverse direction and buffer leakage, a clear field effect with normally-on characteristics was measured in this sample. The threshold voltage of this device is $V_{th}$=-8.6 V measured at $V_{DS}$=10 V by extrapolation of the drain current $I_{DS}$-$V_G$ curve at $V_{DS}$ =10 V shown in Figure 1 (b) indicating normally-on behavior of the device. The measurements of the source and drain contact resistance show a slight non-ohmic behavior which limited the absolute current through the device. Therefore, the source-to-drain current difference between $V_G$=-10 V and $V_G$=4 V was only 80 µA/mm. At high positive gate voltages, an additional gate leakage was observed at low source-to-drain voltages. So, the drain current at $V_G$=4 V is reduced by the gate leakage in forward direction. Additionally, the transconductance $g_m$ of HFET A is depicted in Figure 1 (b).

Capacitance-voltage (C-V) measurements were performed on HFET A at 2 MHz to detect the electron channel at the c-$Al_{0.36}Ga_{0.64}N$/GaN interface. For this purpose, the gate was biased and the source and drain were connected in parallel and grounded. Figure 2 (a) shows the measured room temperature C-V profile of HFET A (blue dots). The typical shape was observed where the capacitance was found to be roughly constant ($V$=0..-1 V) when the electron channel was present, falling to smaller values once the electron channel had been depleted. The left-hand scale is the measured capacity which has been corrected for the parasitic parallel capacity of the $SiO_2$ layer under the contact pads ($C_p$=19.8 pF). The resulting gate capacity is plotted at the right hand-scale. The red dashed curve depicts



Downloaded 22 Dec 2010 to 158.12.36.78. Redistribution subject to AIP license or copyright; see http://proceedings.aip.org/about/rights_permissions

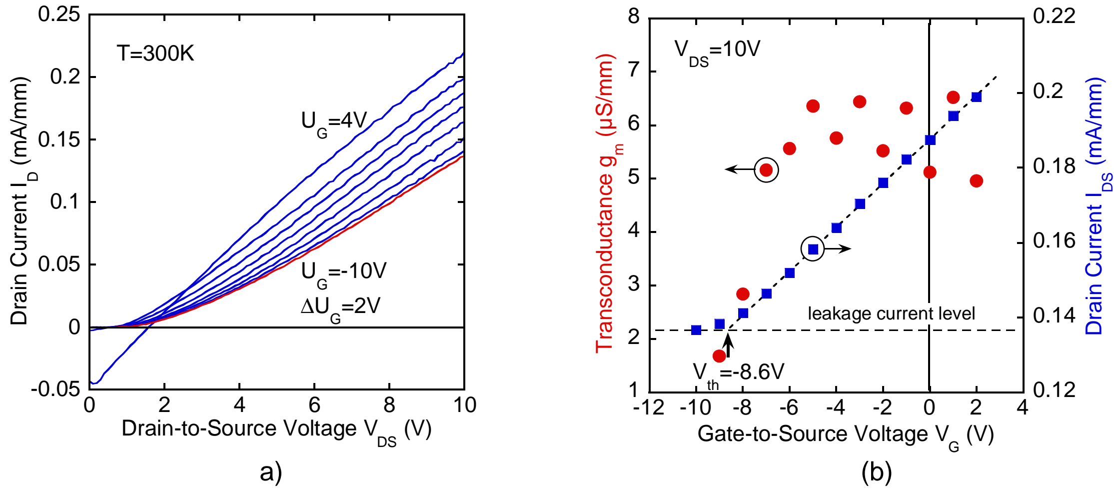


**FIGURE 1.** (a) Static output characteristics of c-AlGaN/GaN HFET A. (b) Transfer characteristics of HFET A at drain-to-source voltage of $V_{DS}$=10 V (blue squares). Also shown is the transconductance as function of the gate voltage (red solid circles).

calculated C-V data of the HFET A using a Poisson-Schrödinger model [16]. For this model calculation a sample structure of 600 nm c-GaN buffer layer with a donor concentration of $N_D=1\times10^{17}$ cm$^{-3}$ followed by a 34 nm c-$Al_{0.36}Ga_{0.64}N$ barrier layer with $N_D=1.5\times10^{18}$ cm$^{-3}$ was used. The assumed Schottky barrier of the gate contact was 0.8 eV.

The C-V data were used to calculate the apparent carrier density $N_{CV}$ in the sample using the following equations [17]:

$$N_{CV} = -\frac{C^3}{q\varepsilon_s A^2}\frac{dV}{dC} \quad (1)$$

$$W_D = \frac{\varepsilon_s A}{C} \quad (2)$$

where $W_D$ is equal to the distance from the surface and $A$ is the contact area. The calculated $N_{CV}$ profiles of the measured (blue dots) and simulated (red dashed line) CV data are depicted in Figure 2 (b). An electron accumulation was observed in the c-GaN layer near the c-$Al_{0.36}Ga_{0.64}N$ /GaN hetero interface with a maximum sheet carrier concentration of $n_{sheet}=1.1\times10^{13}$ cm$^{-2}$ at the c-$Al_{0.36}Ga_{0.64}N$ /GaN interface calculated by the integration of the measured $N_{CV}$ curve.

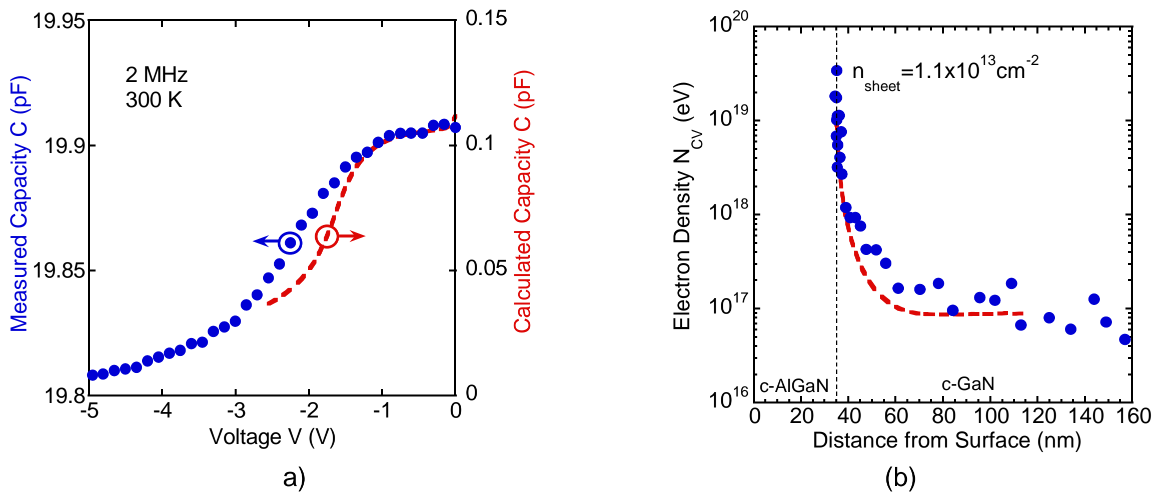


**FIGURE 2.** (a) Measured (blue dots) and calculated (red dashed line) C-V characteristics of HFET A confirming the presence of an electron channel at the c-AlGaN/GaN interface. (b) Measured (blue dots) and calculated (red dashed line) carrier density profile $N_{CV}$ of HFET A.



Downloaded 22 Dec 2010 to 158.12.36.78. Redistribution subject to AIP license or copyright; see http://proceedings.aip.org/about/rights_permissions

## HFET with Normally-off Characteristics

HEFT B with normally-off characteristics consists of 200 nm UID c-GaN on $Ar^+$ implanted 3C-SiC followed by 4 nm UID c-$Al_{0.33}Ga_{0.67}N$ spacer layer, 6 nm thick c-$Al_{0.33}Ga_{0.67}N$:Si doped with $N_D = 4\times10^{18}$ $cm^{-3}$ Si and 10 nm UID c-$Al_{0.33}Ga_{0.67}N$. In this sample, a thinner c-GaN buffer layer was used to minimize the interface roughness between the c-GaN and c-$Al_{0.33}Ga_{0.67}$. Our model calculations show that a buffer leakage through UID c-GaN of 200 nm thickness is insignificant. Thus, a carbon doping of c-GaN for buffer insulation was not necessary. Due to the small c-GaN buffer thickness the RMS roughness of the sample's surface measured by AFM was 3 nm which was lower than that of HFET A. FWHM of the cubic GaN (002) rocking curve was 36 arcmin.

Figure 3 (a) shows the room temperature DC drain IV curves of HFET B. A clear field-effect was measured with this device when the gate voltage was varied from $V_G$=-1 V to $V_G$=2 V. The negative source-drain current at $V_{DS}$=0 V and $V_G$>1 V is induced by gate leakage in forward direction. A parasitic shunt current of 0.34 mA/mm at $V_{DS}$=10 V was observed (red curve) which is caused by reverse gate leakage and an insufficient isolation between the device and high conductive 3C-SiC. The source-to-drain current difference between $V_G$=-1 V and $V_G$=2 V was 0.5 mA/mm.

The transfer characteristics of HFET B are shown in Figure 3 (b). The threshold voltage of the device was $V_{th}$=0.6 V obtained from the intersection of the extrapolated drain current data and the gate leakage line (0.34 mA/mm) revealing that this device is of normally-off type [18]. We had previously reported a cubic AlGaN/GaN HFET in which the electron channel was controlled by positive gate voltage [19]. However, this device offered high parallel conductivity through the 600 nm thick c-GaN buffer layer. With HFET B we demonstrate (i) decreasing of buffer leakage by thinner c-GaN buffer layer and (ii) reproducibility of the normally-off behavior in c-AlGaN/GaN HFETs with similar c-AlGaN barrier layer.

The electron concentration at the c-$Al_{0.33}Ga_{0.67}N$/GaN interface was obtained from C-V measurements which were performed on the gate contact of the device at 2 MHz. Figure 4 (a) shows measured (blue dots) and calculated (red dashed line) C-V characteristics of HFET B confirming the presence of an electron channel at the c-$Al_{0.33}Ga_{0.67}N$/GaN interface. The model calculation was performed using a Poisson-Schrödinger model [16]. The parameters used in the simulation are a 200 nm c-GaN buffer layer with a donor concentration of $N_D=4\times10^{16}$ $cm^{-3}$ followed by a 4 nm c-$Al_{0.33}Ga_{0.67}N$ spacer layer with $N_D=4\times10^{17}$ $cm^{-3}$, a 6 nm layer with $N_D=4\times10^{18}$ $cm^{-3}$, and a 10 nm cap layer with $N_D=4\times10^{17}$ $cm^{-3}$. The measured capacity has been corrected for the parasitic parallel capacity of the $SiO_2$ layer under the contact pads ($C_p$=20.6 pF) and is plotted at the right-hand scale. In contrast to the HFET A the C-V curve of HFET B increases at V>-1 V and depletes at positive voltage around 0.3 V. This is a typical C-V behavior of a normally-off HFET. Figure 4 (b) shows the apparent carrier density $N_{CV}$ of HFET B calculated from the measured C-V characteristics using Equations 1 and 2 (blue dots). The resulting profile shows a carrier accumulation at the c- $Al_{0.33}Ga_{0.67}N$/GaN interface building an electron channel. The red dashed curve is the carrier density calculated from the simulated C-V data of HFET B. The sheet carrier density at the c-$Al_{0.33}Ga_{0.67}N$/GaN interface of the HFET B is with $n_{sheet}=3.4\times10^{12}$ $cm^{-2}$ lower than that of HFET A.

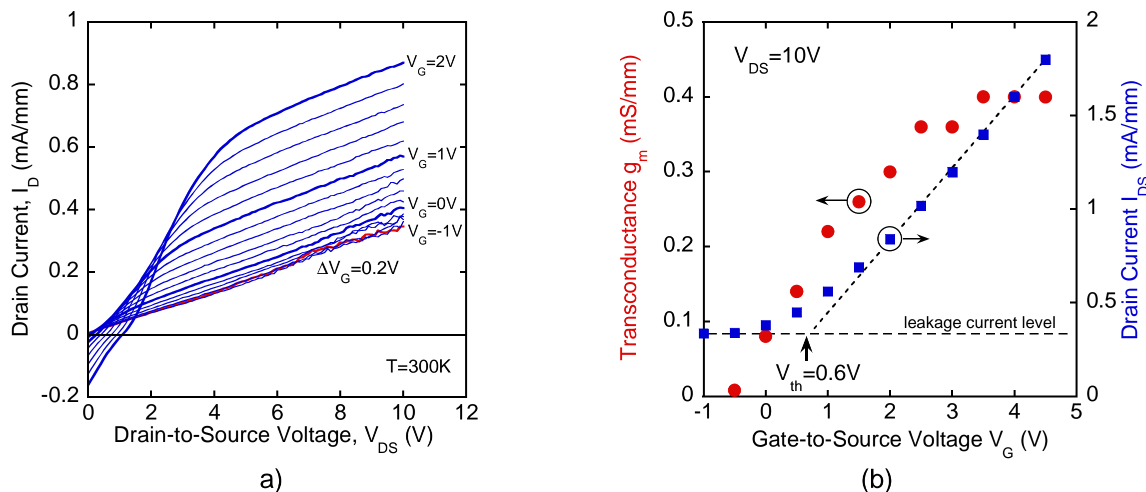


**FIGURE 3.** (a) Static output characteristics of c-AlGaN/GaN HFET B. (b) Transfer characteristics of HFET B at drain-to-source voltage of $V_{DS}$=10 V (blue squares). Also shown is the transconductance as function of the gate voltage (red solid circles).



Downloaded 22 Dec 2010 to 158.12.36.78. Redistribution subject to AIP license or copyright; see http://proceedings.aip.org/about/rights_permissions

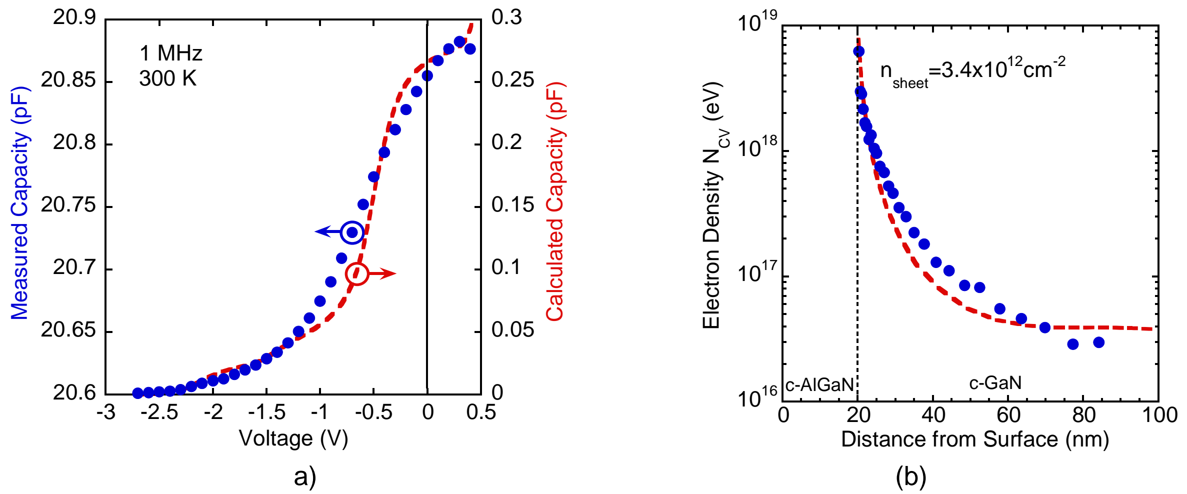


**FIGURE 4.** (a) Measured (blue dots) and calculated (red dashed line) C-V characteristics of HFET B. (b) Calculated (red dashed line) and measured (blue dots) electron concentration $N_{CV}$ of HFET B vs. distance from surface.

## COMPARISON OF POLAR, SEMI-POLAR, AND NONPOLAR ALGAN/GAN HFETS

In Table 1 the experimental data of cubic AlGaN/GaN HFETs A and B are compared with hexagonal polar *c*-plane HFETs and semi-polar *a*-plane HFETs. Due to spontaneous and piezoelectric polarization fields state-of-the-art *c*-plane AlGaN/GaN HFETs are of normally-on characteristics [20]. The maximum source-to-drain current $I_{DS,max}$ of these devices is in the order of some hundred mA/mm. Therefore conventional AlGaN/GaN HFETs are applicable for high-power switching systems. In [21] it was shown that it is possible to fabricate normally-off HFETs of *c*-plane AlGaN/GaN with a thin InGaN cap layer. The polarization-induced field in the InGaN cap layer is expected to raise the conduction band of the AlGaN/GaN interface, which leads to a threshold voltage shift to the positive direction.

However, one way to avoid undesirable polarization fields in HFET devices is the use of semi-polar and non-polar AlGaN/GaN. The first semi-polar HFET of *a*-plane AlGaN/GaN was published in [9]. Compared to *c*-plane HFET the transconductance of *a*-plane devices is lower by a factor of 20-30. This is caused by the still inferior material quality of *a*-plane nitrides and high dislocation density, which reduces the carrier mobility $\mu$ and therefore the transconductance $g_m$. The crystalline quality of non-polar cubic AlGaN/GaN is comparable with that of semi-polar *a*-plane hetero-structures. From the output characteristics of our devices we can estimate the field-dependent electron mobility at the c-AlGaN/GaN interface [22].We find a mobility of about 5 cm$^2$/Vs in the normally-off HFET B. Field-dependent mobility is proportional to the drain current which is limited by high source/drain contact resistance of our devices. Thus, we believe that the real mobility of the electron channel is higher than 5 cm$^2$/Vs. However, the measured value is similar to the Hall mobility of *a*-plane AlGaN/GaN where a maximum mobility of

**TABLE 1.** Comparison of device performance of polar *c*-plane, semi-polar *a*-plane and non-polar cubic AlGaN/GaN HFETs.

| | $L_G$ | $L_{SG}$ | $L_{DG}$ | $V_{th}$ | $I_{DS,max}$ | $g_{m,\ mayx}$ |
|---|---|---|---|---|---|---|
| **normally-on *c*-plane HFET**[20] | 2 µm | 2 µm | 5 µm | -3.5 V | 460 mA/mm at $V_G$=1 V | 125 mS/mm |
| **normally-off *c*-plane HFET with InGaN cap layer** [21] | 1.9 µm | 1.5 µm | 2.4 µm | 0.4 V | 115 mA/mm at $V_G$ =2 V | 85 mS/mm |
| **normally-off *a*-plane HFET in [1-100]** [9] | 1 µm | 2 µm | 2 µm | -0.5 V | 19.5 mA/mm at $V_G$ =1.6 V | 6.7 mS/mm |
| **normally-off *a*-plane HFET in [0001]** [9] | 1 µm | 2 µm | 2 µm | -0.5 V | 13.5 mA/mm at $V_G$ =1.6 V | 3.6 mS/mm |
| **cubic normally-on HFET A** | 2 µm | 3 µm | 3 µm | -8.6 V | 62 µA/mm at $V_G$ =2 V | 6.5 µS/mm |
| **cubic normally-off HFET B** | 2 µm | 3 µm | 3 µm | 0.6 V | 1.4 mA/mm at $V_G$ =4.5 V | 0.4 mS/mm |



Downloaded 22 Dec 2010 to 158.12.36.78. Redistribution subject to AIP license or copyright; see http://proceedings.aip.org/about/rights_permissions

46 $cm^2/Vs$ was measured [9]. A positive threshold voltage $V_{th}$ of 0.6 V was measured on HFET B, whereas for the *a*-plane devices only a "nearly positive" $V_{th}$=-0.5 V was observed. In contrast to hexagonal HFETs, cubic devices show no dependence on the orientation of the gate as observed in *a*-plane HFET in [1-100] and [0001] direction. However, the contact fabrication of cubic AlGaN/GaN HFET devices is not yet optimized. Therefore, the output characteristics of cubic AlGaN/GaN HFET devices are still one order of magnitude lower than those of the *a*-plane HFETs due to high source/drain contact resistance. Additionally, the devices exhibit high off-state conductivity due to high reverse gate conductivity and an insufficient insulation between device and conductive substrate.

## CONCLUSIONS

Hetero-junction field-effect transistors were fabricated of non-polar cubic AlGaN/GaN. These first HFETs show a clear field-effect. However, due to gate and buffer leakage the devices exhibit a residual off-state conductivity. Although the crystalline properties of cubic AlGaN/GaN are comparable with the properties of *a*-plane AlGaN/GaN, the output characteristics of cubic HFETs are still one order of magnitude lower than those of semi-polar devices due to the high source and drain contact resistance. Thus, the contact technology of cubic AlGaN/GaN HFETs has to be improved. The electron channel at the cubic AlGaN/GaN interface of both devices was detected by capacitance-voltage measurements and also verified by calculations using a self consistent Poisson-Schrödinger model. Output and transfer characteristics of cubic AlGaN/GaN HFETs were compared with characteristics of polar *c*-plane und semi-polar *a*-plane devices. Our results demonstrate clearly that cubic AlGaN/GaN can be used for fabrication of HFETs with normally-on and normally-off characteristics.

## ACKNOWLEDGMENTS

The author wants to thank Dr. M. Abe and Dr. H. Nagasawa at HOYA Corporation for the supply of the thick 3C-SiC substrates, Prof. Dr. J.K.N. Lindner for $Ar^+$ implantation of the 3C-SiC substrates. Prof. Dr. D.J. As is acknowledged for the supervision of this work, which was financial supplied by German Science Foundation (DFG, project As (107/4-1).

## REFERENCES


1. S. Rajan, P. Waltereit, C. Poblenz, S.J. Heikman, D.S. Green, J.S. Speck, and U.K. Mishra, IEEE Electron Dev. Lett. **25**(5), 247 (2004).
2. M S. Haffouz, H. Tang, J. A. Bardwell, E.M. Hsu, J.B. Webb, and S. Rolfe, Solid-State Electron. **49**(5), 802 (2005).
3. Y.C. Choi, J. Shi, M. Pophristic, M.G. Spencer, and L.F. Eastman, J. Vac. Sci. Technol. B **25**(6), 1836 (2007).
4. M.A. Khan, Q. Chen, C.J. Sun, J.W. Yang, M. Blasingame, M.S. Shur, and H. Park, Appl. Phys. Lett. **68**(4), 514-516 (1996).
5. Y. Cai, Y. Zhoi, K.M. Lau, and K.J. Chen, IEEE Trans. Electron Dev. **53**(9), 2207-2215 (2006).
6. W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, and I. Omura, IEEE Trans. Electron Dev. **53**(2), 356-362 (2006).
7. M. Ito, S. Kishimoto, F. Nakamura, and T. Mizutani, IEICE Trans. Electron. **E91C**(7), 989 (2008).
8. T. Oka, and T. Nozawa, IEEE Electron Dev. Lett. **29**(7), 668 (2008).
9. M. Kuroda, H. Ishida, T. Ueda, and T. Tanaka, J. Appl. Phys. **102**(9), 093703 (2007).
10. C.Y. Chang, Yu-Lin Wang, B.P. Gila, A.P. Gerger, S.J. Pearton, C.F. Lo, F. Ren, Q. Sun, Yu. Zhang, and J. Han, Appl. Phys. Lett. **95**, 082110 (2009).
11. M. Abe, H. Nagasawa, S. Potthast, J. Fernandez, J. Schörmann, D.J. As, and K. Lischka, IEICE Trans. Electron. **E89**-C, No.7, 1057 (2006).
12. J. Schörmann, S. Potthast, D.J. As, and K. Lischka, Appl. Phys. Lett. **90**, 041918 (2007).
13. E. Tschumak, M.P.F. de Godoy, D.J. As, and K. Lischka, Microelectronics J. **40**(2), 367 (2009).
14. D.J. As, S. Potthast, J. Fernandez, J. Schörmann, K. Lischka, H. Nagasawa, and M. Abe, Appl. Phys. Lett. **88**, 152112 (2006).
15. D.J. As, E. Tschumak, I. Laubenstein, R.M. Kemper, K. Lischka, MRS. Symp. Proc. Vol. **1108**, A01-02 (2009).
16. I.H. Tan, G.L. Snider, L.D. Chang, and E.L. Hu, J. Appl. Phys. **68**(8), 4071 (1990).
17. W.C. Johnson, and P.T. Panousis, IEEE Trans. Electron Dev. ED**18**(10), 965 (1971).
19. E. Tschumak, J.K.N. Lindner, M. Bürger, K. Lischka, H. Nagasawa, M. Abe, and D.J. As, phys. stat. sol. (c), **7**(1), 104-107 (2010).
18. E. Tschumak, R. Granzner, J.K.N. Lindner, F. Schwierz, K. Lischka, H. Nagasawa, M. Abe, and D.J. As, Appl. Phys. Lett. **96**, 253501 (2010).
20. Y.C. Choi, J. Shi, M. Pophristic, M.G. Spencer, and L.F. Eastman, J. Vac. Sci. Technol. B., **25**(6), 1836-1841 (2007).
21. T. Mizutani, M. Ito, S. Kishimoto, and F. Nakamura, IEEE Electron Dev. Lett., 28(7), 549-551 (2007).
22. S.M. Sze and K.K. Ng, Physics of Semiconductor Devices, 3rd ed., Wiley, New Jersey (2007), p. 406.




Downloaded 22 Dec 2010 to 158.12.36.78. Redistribution subject to AIP license or copyright; see http://proceedings.aip.org/about/rights_permissions