Nonpolar cubic AlGaN/GaN heterojunction field-effect transistor on Ar^+ implanted 3C–SiC (001)

E. Tschumak,[1,a)] R. Granzner,[2] J. K. N. Lindner,[1] F. Schwierz,[2] K. Lischka,[1] H. Nagasawa,[3] M. Abe,[3] and D. J. As[1]

[1]*Department of Physics, Faculty of Science, University of Paderborn, Warburger Str. 100, D-33098 Paderborn, Germany*
[2]*FG Festkörperelektronik, TU Ilmenau, Postfach 100565, D-98684 Ilmenau, Germany*
[3]*SiC Development Center, HOYA Corporation, 1-17-16 Tanashioda, Sagamihara, Kanagawa 252-0425, Japan*

(Received 5 November 2009; accepted 27 May 2010; published online 21 June 2010)

A heterojunction field-effect transistor (HFET) was fabricated of nonpolar cubic AlGaN/GaN grown on Ar^+ implanted 3C–SiC (001) by molecular beam epitaxy. The device shows a clear field effect at positive bias voltages with $V_{th}=0.6$ V. The HFET output characteristics were calculated using ATLAS simulation program. The electron channel at the cubic AlGaN/GaN interface was detected by room temperature capacitance-voltage measurements. © *2010 American Institute of Physics*. [doi:10.1063/1.3455066]

AlGaN/GaN heterojunction field-effect transistors (HFETs) are presently of major interest for electronic devices, in particular, for high-power and high-frequency amplifiers. This is motivated by their potential in commercial and military applications, e.g., in communication systems, radar, wireless stations, high-temperature electronics, and high-power solid-state switching. Currently, state of the art HFETs are fabricated of the *c*-plane surface of wurzite (hexagonal) AlGaN/GaN heterostructures. Their inherent spontaneous and piezoelectric polarization fields produce extraordinary large sheet carrier concentrations at the AlGaN/GaN heterointerface. Therefore, all these devices are of the normally-on type.[1–3] However, for switching devices and digital electronics field-effect transistors (FETs) with normally-off characteristics are desirable. Recently AlGaN/GaN HFETs on *c*-plane with normally-off operations[4,5] have been reported. Some groups used nonpolar *a*-plane AlGaN/GaN to fabricate HFETs (Refs. 6 and 7) and demonstrated that the electrical output characteristics of these devices are different for different gate finger orientation on *a*-plane layers. However, up to now no FETs have been realized with nonpolar cubic group III-nitrides although it was discussed recently by Abe[8] that they would offer fabricating HFETs without undesirable parasitic piezoelectric and spontaneous polarization fields and with equal electrical properties for all gate orientations. Further the cubic nitrides would allow using the same technology for normally-on and normally-off devices. In this paper we report the fabrication of HFETs based on cubic III-nitrides. We demonstrate a clear field effect at positive bias voltages with $V_{th}=0.6$ V.

For the epitaxy of our cubic AlGaN/GaN heterostructures freestanding 3C–SiC (001) substrates with a carrier concentration of $n=2\times10^{18}$ cm^{-3}, mobility of $\mu=340$ cm^2/V s and resistivity of $\rho=6.6$ mΩ cm measured by Hall effect were used. A three energy implantation with Ar^+ ions at doses of 6×10^{14} cm^{-2} at 160 keV, 2.4×10^{14} cm^{-2} at 80 keV, and 1.2×10^{14} cm^{-2} at 40 keV was used to form a damage layer near the surface. Transmission electron microscopy investigations of the SiC damage layer showed that after the Ar^+ implantation an amorphous SiC layer beneath the crystalline surface is formed. This layer has identical electrical properties as the bulk 3C–SiC. Thermal annealing at 800 °C leads to recrystallization of the amorphous layer yielding a conductivity decrease in the implanted region by more than two orders of magnitude.[9] Substrates treated in this way allow an effective insulation of the epitaxial c-III-nitride layer from bulk 3C–SiC. Thus, all Ar^+ implanted 3C–SiC substrates have been annealed at 800 °C for 30 min prior to c-AlGaN/GaN epitaxy in order to reduce shunt currents through the substrate.

Cubic AlGaN/GaN heterostructures were grown in a Riber 32 system by plasma-assisted molecular beam epitaxy. In order to minimize hexagonal inclusions in our layers and to obtain an optimum interface roughness, coverage of one monolayer Ga was established during growth.[10] The substrate temperature was 720 °C and the growth rate was 115 nm/h. The c-AlGaN/GaN layer stack consists of 200 nm unintentionally doped (UID) cubic GaN (c-GaN) followed by 4 nm UID cubic $Al_{0.33}Ga_{0.67}N$ (c-$Al_{0.33}Ga_{0.67}N$) spacer layer, 6 nm thick c-$Al_{0.33}Ga_{0.67}N$ doped with $N_D=4\times10^{18}$ cm^{-3} Si and 10 nm UID c-$Al_{0.33}Ga_{0.67}N$. The net donor concentration of reference c-GaN and c-AlGaN layers was measured by capacitance-voltage (CV). It was about 4×10^{16} cm^{-3} for UID c-GaN and one order of magnitude higher for UID c-AlGaN. The root-mean square roughness of the c-$Al_{0.33}Ga_{0.67}N$/GaN surface measured by atomic force microscopy was 3 nm. The dislocation density of c-GaN was about 5×10^9 cm^{-2} as estimated using a relation between the full-width at half maximum of the x-ray rocking curve of the (002) c-GaN reflex and the density of 60° dislocations in cubic structures given by Gay.[11] Thus the crystalline properties of our c-AlGaN/GaN heterostructures were comparable with those of *a*-plane structures.[6]

Ti/Al/Ni/Au (15 nm/50 nm/15 nm/50 nm) was thermally evaporated and annealed at 850 °C for 30 s in nitrogen atmosphere to form source and drain contacts with Ohmic characteristics. Then, c-AlGaN/GaN mesas were formed by $SiCl_4$ reactive ion etching in order to separate single devices.

[a)]Electronic mail: elena.tschumak@uni-paderborn.de.

 © 2010 American Institute of Physics

Downloaded 22 Jun 2010 to 131.234.170.113. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp

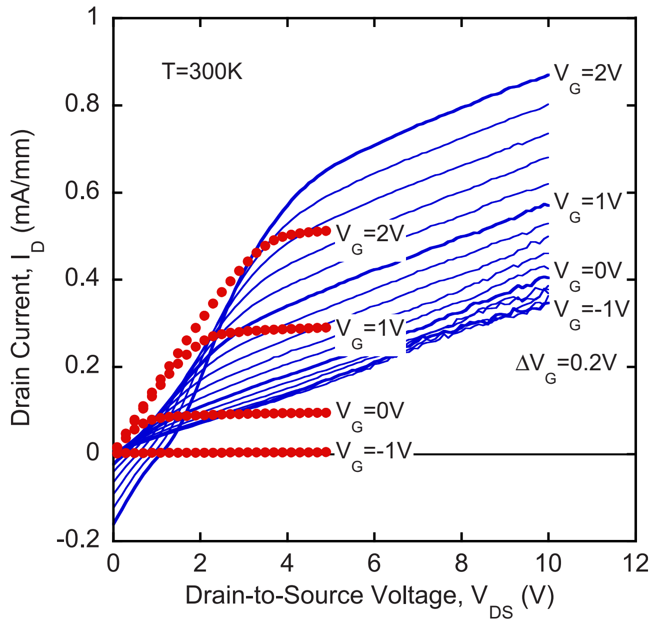

FIG. 1. (Color online) Static output characteristics of a fabricated cubic AlGaN/GaN HFET. The dotted lines represent calculated output characteristics at $V_G=-1$, 0, +1, and +2 V.

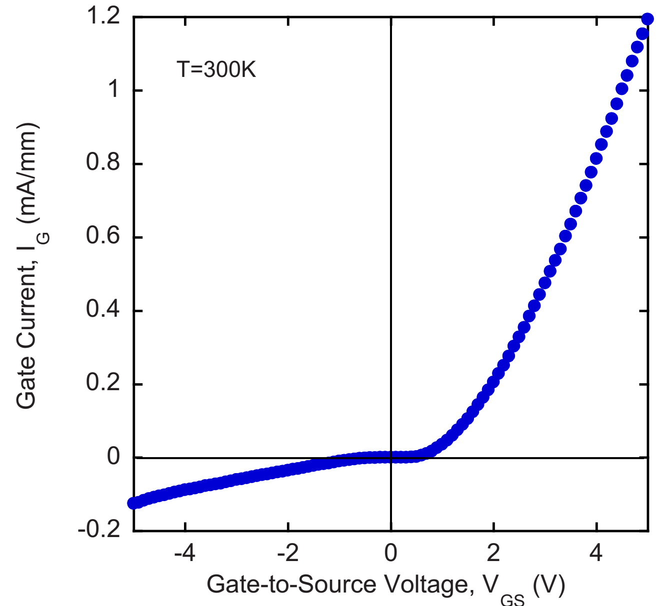

FIG. 2. (Color online) Room temperature IV characteristics of the gate contact.

Gate fingers were fabricated by evaporation of Pd/Ni/Au (15 nm/15 nm/50 nm) and subsequent annealing at 400 °C for 10 min. This procedure decreased the reverse current density of our contacts by more than one order of magnitude. This is in good agreement with earlier findings where it was found that annealing of metal contacts on c-III-nitrides reduces the leakage current significantly.[12,13] Our devices have a gate length of 2 μm, a gate width of 25 μm, and a source-to-drain spacing of 8 μm. Finally, contact pads were thermally evaporated onto a 250 nm thick SiO_2 layer which was deposited around the FET devices for isolation.

Figure 1 shows the room temperature dc drain current-voltage (IV) curves of a c-HFET. A clear field-effect was measured with this device when the gate-to-source voltage was varied from -1 to +2 V. The source-to-drain current difference between $V_G=-1$ V and $V_G=+2$ V was 0.5 mA/mm. This is 20 times lower than the source-to-drain current of *a*-plane AlGaN/GaN HFET with a $[1\bar{1}00]$ gate orientation at $V_G=1.6$ V.[6] We suggest that this difference is mainly due to the lower mobility in our cubic devices and due to the relatively high resistivity of the source and drain contacts of $\rho_C=150$ Ω cm which have not yet been optimized. From the gate contact IV characteristics shown in Fig. 2 we conclude that (i) the negative drain current at $V_{DS}=0$ V and $V_G>1$ V is caused by gate leakage in forward direction and (ii) the drain current of 0.34 mA/mm at $V_{DS}=10$ V and $V_G=0$ V is mainly due to reverse gate leakage ($I_G=0.3$ mA/mm at $V_{DS}=10$ V and $V_G=0$ V). From the output characteristics of our device we can estimate the field-depend electron mobility at the c-AlGaN/GaN interface.[14] We find a mobility of about 5 cm^2/V s. This value is limited mainly by the dislocation density and the interface roughness as shown in Ref. 15 for cubic and in Ref. 16 for hexagonal AlGaN/GaN. It is similar to the Hall mobility of *a*-plane AlGaN/GaN where a maximum mobility of 46 cm^2/V s was measured.[6]

The output characteristics of our device were calculated with the two-dimensional device simulator ATLAS.[17] The parameters used in the simulation are a 3C–SiC substrate with zero conductivity followed by 200 nm c-GaN buffer layer, a 4 nm c-$Al_{0.33}Ga_{0.67}N$ spacer layer with $N_D=4\times10^{17}$ cm^{-3}, a 6 nm layer with $N_D=4\times10^{18}$ cm^{-3}, and a 10 nm cap layer with $N_D=4\times10^{17}$ cm^{-3}. A donor concentration of $N_D=4\times10^{16}$ cm^{-3} and an electron mobility of $\mu=5$ cm^2/V s in the c-GaN layer at the c-AlGaN/GaN interface was assumed. Further a linear decrease in the donor concentration and mobility with increasing distance from the surface had to be taken into account to fit best the experimental data. This assumption seems reasonable since it has been shown in Ref. 18 that the dislocation density of c-GaN layers increases with decreasing distance to the substrate-layer interface. The contact resistivity of the source and drain contacts was set to $\rho_C=150$ Ω cm. The Schottky gate contact with a barrier height of 0.8 eV was localized on top of the c-AlGaN layer. Like in the realized HFET devices the gate length was 2 μm and the gate-to-source and gate-to-drain spacing was 3 μm. However, it was not possible to include the effect of gate leakage in the simulation.

The dotted lines in Fig. 1 represent the calculated drain current I_D of our HFET at $V_G=-1$ V, 0 V, 1 V, and 2 V, respectively. The increase in the calculated drain current with increasing V_G is in good agreement with the measured data. However, experimental data show a drain current at $V_G=0$ V which is not found in the simulation. Thus we conclude that the measured drain current is due to gate leakage in reverse direction.

The measured (squares, left-hand scale) and calculated (circles, right-hand scale) transfer characteristics of the cubic HFET at $V_{DS}=10$ V are depicted in Fig. 3. The calculated data are shifted with respect to the experimental data since we belief that the current measured at $V_G=-1$ V is mainly due to gate leakage which has not been included in the simulation. The threshold voltage $V_{th}=0.6$ V was obtained from the intersection of the extrapolated experimental drain current data and the gate leakage line (0.34 mA/mm). Thus, the electron channel at c-AlGaN/GaN interface is controlled by positive gate bias.

Downloaded 22 Jun 2010 to 131.234.170.113. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp

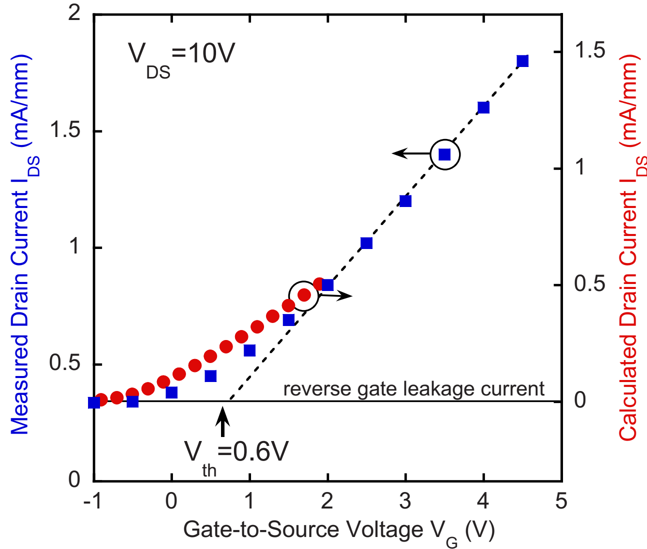

FIG. 3. (Color online) Measured (squares) and calculated (solid circles) transfer characteristics of a cubic $Al_{0.33}Ga_{0.67}N/GaN$ HFET at drain-to-source voltage of $V_{DS}=10$ V. The right-hand scale of the calculated data is shifted for the value of the reverse gate leakage current of 0.34 mA/mm measured at $V_G=-1$ V.

The electron concentration at the c-AlGaN/GaN interface was obtained from CV measurements which were performed at 1 MHz. For this purpose, the gate was biased and source and drain were connected in parallel and grounded. The CV data were used to calculate the apparent carrier density N_{CV} in the sample using the following equations:[19]

$$N_{CV} = -\frac{C^2}{e\varepsilon\varepsilon_0 A^2}\frac{dV}{dC}, \quad (1)$$

$$z_{CV} = \frac{\varepsilon\varepsilon_0 A}{C}, \quad (2)$$

where z_{CV} is equal to the distance from the surface and A is the contact area. The resulting carrier N_{CV} profile is depicted in Fig. 4 (solid dots). It is superimposed to the conduction band edge of the device calculated using a Poisson–Schrödinger model.[20] In the calculation we set $V_G=0.3$ V. At this gate voltage the highest carrier concentration of $N_{CV}=6\times10^{18}$ cm^{-3} at the c-AlGaN/GaN interface was measured. The dashed curve shows the calculated carrier density profile. An electron channel at the c-AlGaN/GaN interface with a sheet carrier density of $n_{sh}=1.7\times10^{12}$ cm^{-2} calculated by the integration of the measured N_{CV} curve is found.

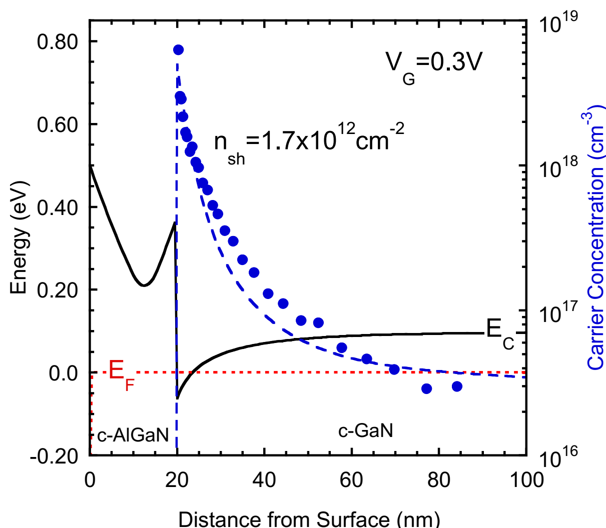

FIG. 4. (Color online) Calculated conduction band edge (solid curve), calculated (dashed curve), and measured (solid dots) electron concentration vs distance from surface.

In conclusion, we have fabricated a heterojunction FET of nonpolar cubic AlGaN/GaN deposited on Ar^+ implanted 3C–SiC (001). Our device shows a clear field-effect and the electron channel at the c-AlGaN/GaN interface is controlled by positive gate voltage with $V_{th}=0.6$ V. However due to gate leakage the device did not yet exhibit the characteristics of an ideal normally-off FET. The electron sheet density in the channel was obtained from CV measurements to be $n_{sh}=1.7\times10^{12}$ cm^{-2} at the c-AlGaN/GaN interface. Simulated output characteristics are in good agreement with our experimental results revealing that the shunt current is mainly due to gate leakage. Our results demonstrate clearly that cubic AlGaN/GaN can be used for fabrication of HFETs with normally-off characteristics.

This work was financially supported by the German Science Foundation (DFG, Project Nos. As 107/4-1 and SCHW 729/7-1) and the University of Paderborn.

[1]S. Rajan, P. Waltereit, C. Poblenz, S. J. Heikman, D. S. Green, J. S. Speck, and U. K. Mishra, IEEE Electron Device Lett. **25**, 247 (2004).
[2]S. Haffouz, H. Tang, J. A. Bardwell, E. M. Hsu, J. B. Webb, and S. Rolfe, Solid-State Electron. **49**, 802 (2005).
[3]Y. C. Choi, J. Shi, M. Pophristic, M. G. Spencer, and L. F. Eastman, J. Vac. Sci. Technol. B **25**, 1836 (2007).
[4]M. Ito, S. Kishimoto, F. Nakamura, and T. Mizutani, IEICE Trans. Electron. **E91-C**, 989 (2008).
[5]T. Oka and T. Nozawa, IEEE Electron Device Lett. **29**, 668 (2008).
[6]M. Kuroda, H. Ishida, T. Ueda, and T. Tanaka, J. Appl. Phys. **102**, 093703 (2007).
[7]C. Y. Chang, Y.-L. Wang, B. P. Gila, A. P. Gerger, S. J. Pearton, C. F. Lo, F. Ren, Q. Sun, Yu. Zhang, and J. Han, Appl. Phys. Lett. **95**, 082110 (2009).
[8]M. Abe, H. Nagasawa, S. Potthast, J. Fernandez, J. Schörmann, D. J. As, and K. Lischka, IEICE Trans. Electron. **E89-C**, 1057 (2006).
[9]E. Tschumak, M. P. F. de Godoy, D. J. As, and K. Lischka, Microelectron. J. **40**, 367 (2009).
[10]J. Schörmann, S. Potthast, D. J. As, and K. Lischka, Appl. Phys. Lett. **90**, 041918 (2007).
[11]P. Gay, P. B. Hirsch, and A. Kelly, Acta Metall. **1**, 315 (1953).
[12]D. J. As, S. Potthast, J. Fernandez, J. Schörmann, K. Lischka, H. Nagasawa, and M. Abe, Appl. Phys. Lett. **88**, 152112 (2006).
[13]D. J. As, E. Tschumak, I. Laubenstein, R. M. Kemper, and K. Lischka, *Performance and Reliability of Semiconductor Devices*, MRS Symposia Proceedings Vol. 1108 (Materials Research Society, Pittsburgh, 2009), pp. A01–02.
[14]S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. (Wiley, New Jersey, 2007), p. 406.
[15]S. Potthast, Growth and characterization of cubic AlGaN/GaN based devices, PhD thesis, University of Paderborn, 2006.
[16]D. Jena, I. Smorchkova, A. C. Gossard, and U. K. Mishra, Phys. Status Solidi B **228**, 617 (2001).
[17]ATLAS User's Manual—Device Simulation Software, Salvaco International, 2008.
[18]D. J. As, S. Potthast, J. Schörmann, S. F. Li, K. Lischka, H. Nagasawa, and M. Abe, Mater. Sci. Forum **527–529**, 1489 (2006).
[19]W. C. Johnson and P. T. Panousis, IEEE Trans. Electron Devices **18**, 965 (1971).
[20]I. H. Tan, G. L. Snider, L. D. Chang, and E. L. Hu, J. Appl. Phys. **68**, 4071 (1990).

Downloaded 22 Jun 2010 to 131.234.170.113. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp