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Insulating substrates for cubic GaN-based HFETs

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ABSTRACT

The growth of cubic group III-nitrides is a direct way to eliminate polarization effects, which inherently limits the fabrication of normally off heterojunction field-effect transistors (HFETs) in the GaN technology. However, for the achievement of electronic devices with cubic nitrides an important precondition is the availability of a high-resistive substrate or GaN buffer layer with zinc-blende crystal structure. We investigated the applicability of carbonized high resistance Si (0 0 1)-substrates and thick conductive free-standing 3C-SiC (1 0 0) substrates with an Ar^{+}-ion-damaged surface layer for this purpose and studied the use of carbon-doped GaN buffer layers for electrical insulation. We found that Ar-implantation of 3C-SiC is an appropriate alternative to fabricate insulation layer for cubic GaN (c-GaN) growth and that C-doped GaN buffers introduce non-linear *I–V* characteristics. The structural properties of c-GaN on Ar-implanted 3C-SiC are comparable to GaN on untreated 3C-SiC whereas on carbonized Si substrates an increase of dislocation density and surface roughness is observed.

1. Introduction

AlGaN/GaN heterojunction field-effect transistors (HFETs) are presently of outstanding interest for electronic devices, in particular, for high-power and high-frequency amplifiers. This is motivated by the potential commercial and military field application, namely, in the area of communication systems, radar, wireless stations, high-temperature electronics and high-power solid-state switching [1,2]. Currently, most of the reported AlGaN/GaN HFETs are fabricated on *c*-plane faces of the stabile wurzite (hexagonal) crystal structure with inherent spontaneous and piezoelectric polarization fields which produce extraordinarily high sheet carrier concentration at the heterointerface. Therefore, all these devices are of the normally on variation [3,4]. Kuroda et al. [5] realized a non-polar *a*-plane AlGaN/GaN HFET with nearly normally off operation in which the threshold voltage is $-0.5\,V$ [5]. However, group III-nitrides can also crystallize in a metastable zinc-blende (cubic) lattice structure free from parasitic built-in polarization field which affords to fabricate a normally off HFET. An important condition to achieve this device is a high-resistive substrate or GaN buffer layer to ensure proper drain–source saturation, complete channel pinch-off, and low loss at high frequencies.

In this article, we discuss several options to reduce the parallel conductivity for HFET applications. We report on crystallographic and electrical properties of cubic GaN grown on semi-insulating carbonized Si (3C-SiC/Si) [6], on free-standing thick conductive 3C-SiC substrates and on Ar-implanted 3C-SiC substrates. Since it is well known that the semi-insulating hexagonal GaN on sapphire and Si (1 1 1) substrates can be achieved by means of carbon doping [3,7] we additionally studied the possibility to use carbon-doped cubic GaN buffer layers for electrical insulation.

2. Experiment

All samples were grown in a Riber 32 system by plasma-assisted molecular beam epitaxy (MBE) under well-controlled growth conditions using a Ga coverage of 1 monolayer. The optimized growth conditions for cubic GaN were described elsewhere [8,9]. In order to study several possibilities to reduce the parasitic parallel conductivity, three different substrates were used. Fig. 1 shows a schematical cross-section of the fabricated samples.

The first substrate was a 3-nm-thick 3C-SiC (0 0 1) on highly isolating Si with a specific resistance of $2\times10^{4}\,\Omega\,cm$. Six hundred nanometer thick cubic GaN (c-GaN) film was grown on this substrate [10] without intentionally doping during growth (Sample A).

For the second sample we used 200-μm-thick free-standing 3C-SiC (0 0 1) substrates with a nominal specific resistance of $6.6\times10^{-3}\,\Omega\,cm$. For electrical insulation these free-standing 3C-SiC substrates were Ar^{+} ion implanted to generate an ion-damaged insulation layer just beneath the surface. Using a 3-fold implantation of Ar^{+}-ions with energies and doses of 160 keV, $6\times10^{14}\,at/cm^{2}$, 80 keV, $2.4\times10^{14}\,at/cm^{2}$, 40 keV, $1.2\times10^{14}\,at/cm^{2}$, respectively, TRIM implantation profile calculations proposed

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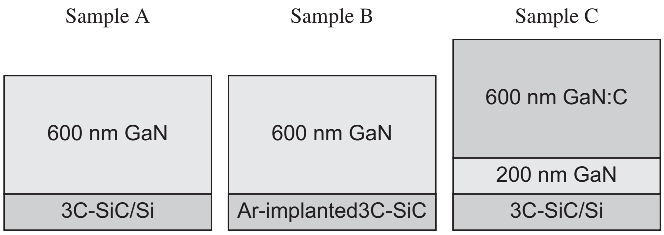

Fig. 1. Schematic cross-section of the fabricated sample structures.

a 200-nm-thick highly damaged layer about 50 nm below the surface. Contact resistance measurements by a four-probe technique indicated a clear increase of resistance from <1 kΩ to ~100 kΩ. Such a layer has to fulfil three criteria. First, the cubic crystal lattice structure has to be preserved, which means that the ion-implantation dose has to be below the dose of amorphization. Second, the implantation elements have to be neutral and the damage has to compensate the high n-type conductivity of the as grown substrate. The third criterion is that the damage has to be resistant against thermal annealing during the time of MBE growth of the c-GaN epilayers (at least 10 h at a temperature of about 800 °C). Likewise on the Ar-implanted 3C-SiC 600 nm undoped c-GaN was deposit by MBE (Sample B).

The third substrate was a 200-μm-thick free-standing 3C-SiC (0 0 1) substrates with a nominal specific resistance of 6.6×10^{-3} Ω cm. Two hundred nanometer undoped GaN followed by 600 nm carbon-doped c-GaN (c-GaN:C) were deposited by MBE (Sample C). The carbon source was a home-made carbon tetra-bromide (CBr_4) sublimation source. The CBr_4 flux was preset by a needle valve to 4.6×10^{14} cm^{-2} s^{-1}. Structural characterization of the samples was carried out by high-resolution X-ray diffraction (HRXRD) and the surface roughness was investigated by atomic force microscopy (AFM). For electrical measurements Ti/Al/Ni/Au (10/25/10/50 nm) ohmic contacts with a diameter of 300 μm were produced by thermal evaporation. Prior to metallization the c-GaN surfaces were cleaned by acetone, propanol and a buffered oxide etch (BOE). The backside of the 3C-SiC substrates were contacted to a copper board using Indium.

3. Results and discussion

HRXRD ω-scans of the (0 0 2) Bragg reflection of the GaN layers were taken in order to evaluate the crystalline quality of the samples. Typical results from the undoped c-GaN on 3C-SiC/Si and on Ar-implanted 3C-SiC and of carbon-doped c-GaN on 3C-SiC are shown in Fig. 2. The full-width at half-maximum (FWHM) are 61, 27 and 15 arcmin, respectively. The linewidth measured for c-GaN grown on thick free-standing 3C-SiC substrates is approximately a factor of three narrower than that for layers grown on carbonized Si substrates. This may be expected due to the low lattice mismatch of the c-GaN/3C-SiC system of only −3.7%. For the GaN/Si system, which is relevant for the carbonized Si substrate, the lattice mismatch is +16,8%. By using the model of Ayers [11], which correlates X-ray FWHM to dislocation density N_{disl}, a dislocation density of about 2×10^{9} cm^{-2} is estimated for c-GaN epilayers on 3C-SiC. For c-GaN on carbonized Si the dislocation density is an order of magnitude higher. In addition to the broader rocking curve the amount of crystalline quality is reduced and the surface roughness is increased. The amount of hexagonal inclusions, determined from reciprocal space maps (not shown here) is up to 13% for GaN grown on 3C-SiC/Si, whereas it is below 1.5% in GaN grown on 3C-SiC or Ar-implanted 3C-SiC and is nearly independent of wheather the c-GaN is nominally undoped or C-doped. The RMS roughness measured by a 5×5 μm^2 AFM scan

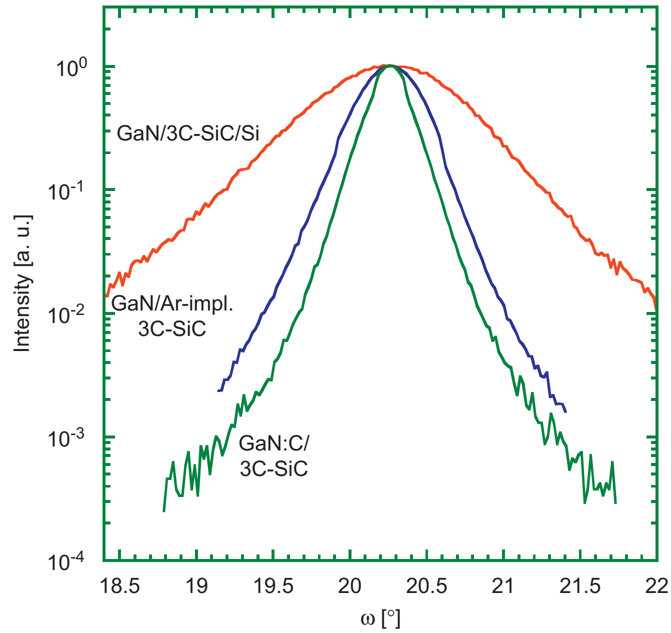

Fig. 2. HRXRD ω-scans of the symmetric (0 0 2) reflection of cubic GaN for three investigated samples.

Table 1
FWHM of HRXRD ω-scans, RMS roughness and hexagonal inclusions of c-GaN on 3C-SiC/Si, on Ar-implanted 3C-SiC and of c-GaN:C on 3C-SiC

Sample	FWHM of ω-scan (arcmin)	RMS roughness 5×5 μm^2 (nm)	Inclusions h-GaN (%)
A	61	13	13
B	27	12	<1.5
C	15	6	<1.5

is 13, 12 and 6 nm for c-GaN grown on 3C-SiC/Si, on Ar-implanted 3C-SiC and for GaN:C on 3C-SiC, respectively. The results of the structural characterization are summarized in Table 1. They indicate that both the structural quality and the surface roughness of the c-GaN layer grown on carbonized 3C-SiC/Si substrate (Sample A) are insufficient for c-GaN-based HFET applications. However, GaN on Ar-implanted 3C-SiC (Sample B) and GaN:C on 3C-SiC (Sample C) exhibit good crystalline quality.

Therefore, we further investigated only the electrical properties of the Samples B and C. The result of both efforts is documented in Fig. 3, which shows the *I–V* characteristics measured between Ti/Al/Ni/Au contact on top and Indium contact on sample backside of an undoped c-GaN layer on Ar-implanted 3C-SiC (blue squares) and of a carbon-doped GaN layer on untreated 3C-SiC (green diamonds). For comparison an undoped c-GaN layer on untreated 3C-SiC is also depicted (full red dots). At -4 V, the current density through the undoped c-GaN on 3C-SiC is 100 times higher than that through the undoped c-GaN layer on the Ar-implanted 3C-SiC and 500 times higher than that through GaN:C on the same substrate. However, the *I–V* characteristics of the C-doped GaN buffer layer shows a non-linear behaviour, and the current flow at a positive bias of +4 V is higher than that of the Ar-implanted substrate. This asymmetric behaviour of the *I–V* curve measured for the carbon-doped GaN layer will be investigated in more details in a future study. From this study, we conclude that Ar-implanted SiC-sample shows the best insulation in both current flow directions and the ion-implantation

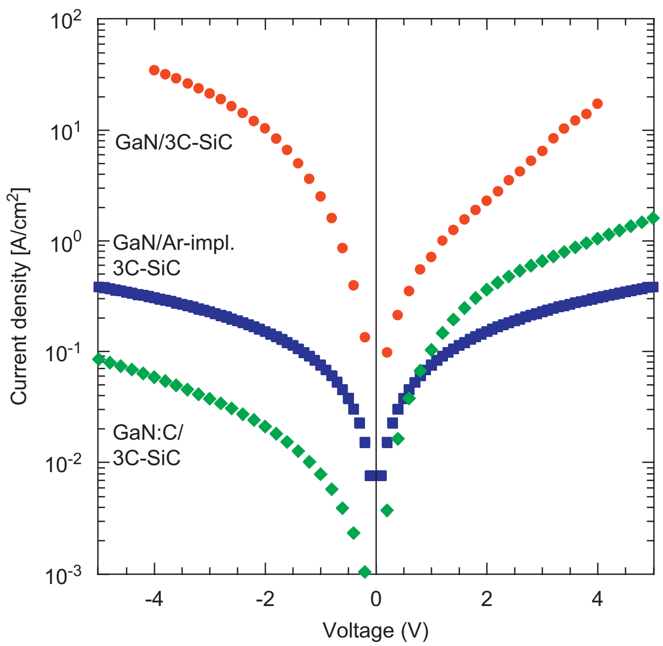

Fig. 3. *I–V* characteristics (log scale) of nominally undoped c-GaN on as grown 3C-SiC and on Ar-implanted 3C-SiC and *I–V* curve of carbon-doped c-GaN on as grown 3C-SiC substrates measured between Ti/Al/Ni/Au contact on top and Indium contact on sample backside.

damage is resistant against thermal annealing during the time of MBE growth.

4. Conclusion

We demonstrate that both the generation of an ion-damaged insulation layer just beneath the surface of free-standing thick 3C-SiC substrate or the growth of a C-doped GaN buffer layer are suitable ways to insert an electrical insulation between the active device area and the conductive 3C-SiC substrate for future electronic devices based on cubic group III nitrides. In both cases the crystalline quality and phase purity of the overgrown cubic GaN epilayer is not deteriorated, whereas the vertical current density is reduced by several orders of magnitude. For high-resistive-carbonized Si (0 0 1) substrates, the X-ray rocking curve of cubic GaN epilayers is broadend by a factor of three indicating an increased dislocation density and is accompanied by additonal surface roughening.

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