

Electrical characterization of an interface n-type conduction channel in cubic GaN/AlGa_{1-x}N heterostructures

A. Zado*, E. Tschumak, K. Lischka, and D. J. As**

Department of Physics, University of Paderborn, Warburger Str. 100, 33095 Paderborn, Germany

Received 20 June 2009, revised 1 August 2009, accepted 4 August 2009

Published online 9 December 2009

PACS 61.05.cp, 68.37.Ps, 68.55.ag, 73.40.Qv, 81.05.Ea, 81.15.Hi

* Corresponding author: e-mail: azado@mail.uni-paderborn.de

** e-mail: d.as@uni-paderborn.de

We report on the growth of non-polar cubic GaN/Al_xGa_{1-x}N hetero-structures by plasma-assisted molecular beam epitaxy on free standing (001) 3C-SiC substrates. The samples consist of 600 nm thick GaN buffer and 30 nm Al_xGa_{1-x}N layer. The growth was observed by in-situ reflection high energy electron diffraction (RHEED). Layer thickness was determined by Al_xGa_{1-x}N RHEED growth oscillations and by reflectance measurements after growth. The morphological and the structural properties are analyzed by high resolution x-ray diffraction (HRXRD) and atomic force microscopy (AFM). Using a metal oxide semiconductor heterostructure (MOSH), capaci-

tance voltage (CV) characteristics were measured. The oxide layer consists of SiO₂, the thickness was varied between 15 nm and 30 nm. SiO₂ layer was produced by plasma enhanced chemical vapour deposition (PECVD). The contact structure is lithographically deposited on top of the sample. Metal contacts have a diameter of 300 μm and were thermally evaporated consisting of 15 nm Ni and 50 nm Au. By CV measurements of the MOSH structures we obtain clear evidence for the existence of an electron accumulation layer at the GaN/AlGa_{1-x}N interface. The sheet carrier concentration at the hetero-interface is calculated from experimental data.

© 2010 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

1 Introduction The reduction of dimensions in electronic devices like high electron mobility transistors may allow higher transfer rates in data communication systems. III-nitride based high electron mobility transistors (HEMT) have exhibited great potential for high-frequency and high-power applications. Under equilibrium conditions, gallium nitride (GaN) crystallizes in the hexagonal (wurtzite) structure. Growth along the polar c-axis leads to strong internal electric fields, which may limit the switching time of devices. The growth of nonpolar cubic group III-nitrides on (001) oriented substrates is a direct way to eliminate these polarization fields [1].

However, the most important feature of high power devices is an n-type conduction channel formed at the heterostructure interface. An outstanding method of electrical investigation of such an electron conduction channel is given by capacitance voltage characterization.

2 Experimental details

2.1 Growth of GaN/Al_xGa_{1-x}N heterostructures

The optimum conditions for the epitaxial growth of c-GaN and c-Al_xGa_{1-x}N are mainly determined by two parameters, namely the surface stoichiometry and the substrate temperature [2]. Both parameters are interrelated, therefore an in-situ control of both substrate temperature and surface stoichiometry is necessary. This is achieved by monitoring growth process by reflection high energy electron diffraction (RHEED) [3]. The heterostructures were grown by plasma assisted molecular beam epitaxy (PAMBE) at 720 °C on free standing 3C-SiC in (001) direction. A 600 nm thick c-GaN buffer layer was deposited on the substrate. On top of the GaN buffer a 30 nm thick c-Al_xGa_{1-x}N layer was grown. The layer thickness was measured in-situ by RHEED oscillations and ex-situ by reflectance measurements. The structural properties of the samples were characterized by high resolution x-ray diffraction (HRXRD) measurements.

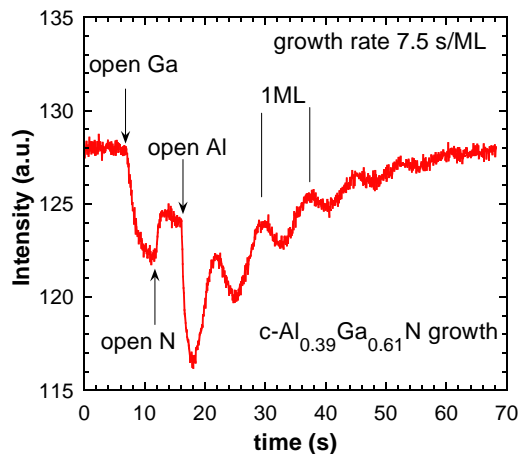


Figure 1 RHEED intensity vs. time during the initial growth of cubic $\text{Al}_{0.39}\text{Ga}_{0.61}\text{N}$. The oscillations indicate a two dimensional growth mode with a rate of 7.5 s/ML.

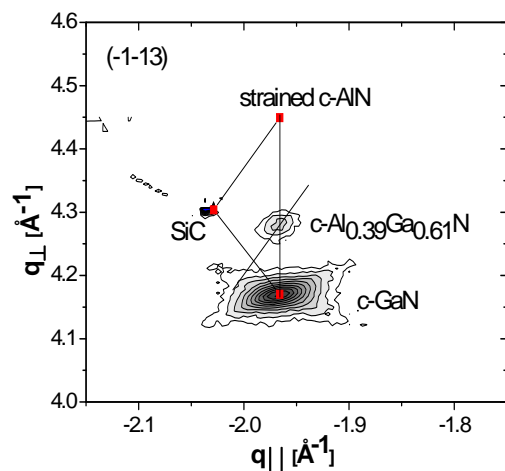


Figure 2 Reciprocal space map around the (-1-13) reflex, intensity of the GaN buffer layer, the $\text{Al}_{0.39}\text{Ga}_{0.61}\text{N}$ film and the SiC substrate are obtained.

From the full width of half maximum (FWHM) of the reflex perpendicular to the surface, the density of defects can be evaluated. Reciprocal space mapping (RSM) gives a two-dimensional distribution of the intensity. In case of scanning around an asymmetric lattice point, information about the strain status and the composition of ternary alloys of the layers are observed. Figure 1 shows a time-scan of RHEED intensity during the initial growth of $\text{c-Al}_{0.39}\text{Ga}_{0.61}\text{N}$. The intensity oscillations indicate a growth of a smooth two dimensional surface. From the oscillation period a growth rate of 7.5 s/ML was determined. Figure 2 shows a RSM around the asymmetric (-1-13) reflex of the grown sample. The map contains two important informations. The first one is that the 30 nm thick AlGa_{0.39}N layer is pseudomorph on the GaN buffer and the second information is the Aluminium mole fraction of 0.39.

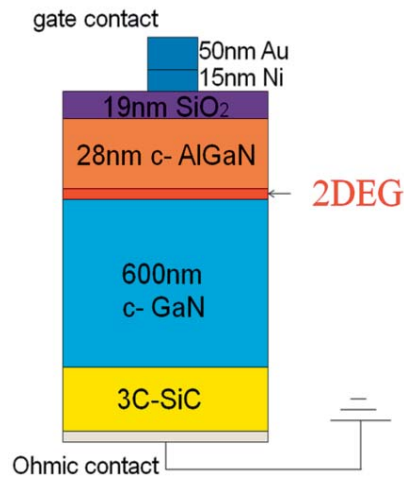


Figure 3 Sample structure with a SiO_2 layer on top of cubic AlGa_{0.39}N/GaN. Ni/Au metal gate contacts on top and Ohmic contact on the backside of the sample

2.2 C-V measurements at MOSH structures The SiO_2 layer was deposited by plasma enhanced chemical vapour deposition in a PECVD system from Oxford Instruments. The basic process for deposition of SiO_2 films in the “Plasmalab PECVD System 100” uses a mixture of 5% silane diluted in nitrogen as the silicon source, and nitrous oxide as the oxygen source. In Table 1 the process parameters are shown.

Table 1 PECVD process parameter range.

Parameter	Values
5% SiH_4 / 95% N_2 flow	30 sccm
N_2O flow	700 sccm
Pressure	400 mTorr
R.F. power*	5 W at 13.56 MHz
Temperature	300 °C

*Strike power 25 W (then ramp down 15 W, 10 W, 5 W)

Using standard lithography the round contact structures with a diameter of 300 μm were placed on the top of the oxide layer. Metal gate contacts were thermally evaporated consisting of 15 nm Ni and 50 nm Au. Figure 3 shows the grown sample structure with a 30 nm SiO_2 film on top of the AlGa_{0.39}N layer. The Ohmic contact was realized by soldering the SiC on a Cu plate with In. The CV measurements were done with the Agilent E4980A universal-LCR-Meter. On the gate contact, a direct voltage in a range between -5 V and +2 V was applied. The Ohmic contact at the backside of the sample was grounded. The amplitude of the alternating voltage was 50 mV and the frequency was 2 MHz.

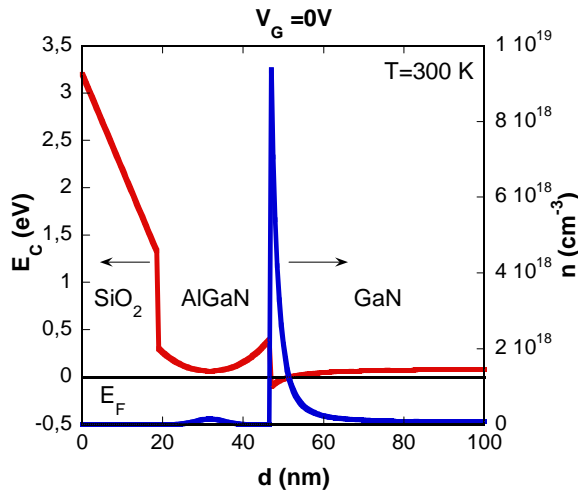


Figure 4 Calculated conduction band-edge and the electron concentration versus thickness d at 0V gate voltage using the PSM.

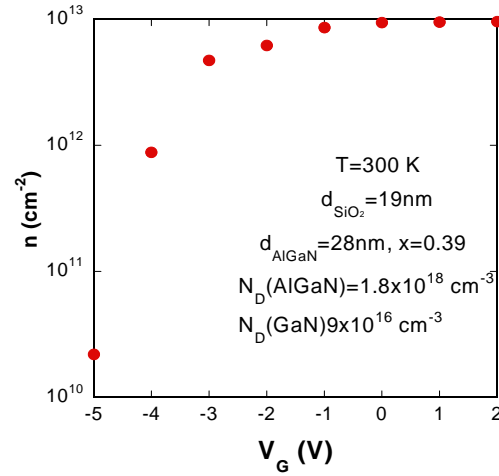


Figure 5 The calculated sheet carrier concentration at the GaN/AlGaN heterointerface as a function of the applied gate voltage using PSM

3 Theoretical calculations To calculate the band structure and the charge carrier distribution a self consistent one dimensional Poisson-Schrödinger Model (PSM) was used [4]. In one dimension the Poisson equation is reduced to:

$$\frac{\partial^2}{\partial x^2} \Phi(x) = -\frac{\rho(x)}{\epsilon_0 \epsilon_r} \quad (1)$$

Figure 4 shows the calculated conduction band-edge and the charge carrier distribution of the measured sample. These two parameters are plotted as a function of the distance d from the surface. Due to the conduction band bending an accumulation layer with a sheet concentration of $9.4 \times 10^{12} \text{ cm}^{-2}$ is formed at the GaN/AlGaN heterointerface. By applying a negative gate voltage the channel depletes. From PSM the calculated sheet carrier concentration is plotted as a function of the applied gate voltage. By increasing the negative voltage the carrier concentration decreases. In case of positive gate voltage the carrier concentration saturates and amounts at about $9.6 \times 10^{12} \text{ cm}^{-2}$.

PSM can also be used to calculate the capacitance as a function of the applied gate voltage. The capacitance of an arbitrary charge distribution is expressed in following equation.

$$C = \epsilon_0 \epsilon_r \frac{\oint \vec{E} d\vec{A}}{\int \vec{E} d\vec{s}} \quad (2)$$

The numerator expresses the total electric charge of the system as an integral of the electric field over a closed area. The denominator is the electric potential represented by the path integral over the electric field.

PSM calculates the capacitance per square centimetre, in one dimension Eq. (2) simplifies to:

$$\frac{C}{A} = \epsilon_0 \epsilon_r \frac{E_x}{\int E_x dx} \quad (3)$$

The x-component from the electric field is well known from Eq. (1). The second spatial derivation of electric potential has only been substituted by negative first spatial derivation of the electric field. Figure 5 shows the 2-dimensional charge carrier concentration vs. gate voltage calculated from PSM.

4 Results and discussion Cubic GaN/AlGaN hetero structures were grown by PAMBE on free standing SiC at 720 °C. A MOSH configuration was realized by depositing an SiO₂ layer on top of the sample. Metal Ni/Au gate contacts were thermally evaporated. A measured C-V curve of the structure depicted in Fig. 3 is shown in Fig. 6.

By decreasing the gate voltage the depletion zone increases, so the C-V measurement gives a depth profile of the sample. The C-V curve consists of three main parts. These parts are referred to the AlGa_N, the GaN and the electron accumulation layer.

The range from -1.0 V to -1.9 V belongs to the 28 nm thick Al_{0.39}Ga_{0.61}N layer. The form of this range depends on the donor concentration in the AlGa_N sheet and the Al content. The region of the most interest is between -1.9 V and -3.4 V gate voltage. This section is referred to the electron conduction channel. The capacitance is almost constant or changes slightly in this voltage region. This behaviour is caused by the charge carrier concentration localized at the heterointerface. From Eq. (4) the charge carrier concentration at the heterointerface can be calculated [5].

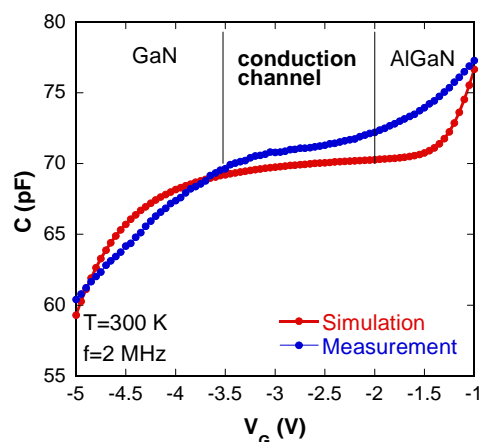


Figure 6 Measured C-V curve of the sample shown in Fig. 3 (empty circles) and a simulated curve by PSM (filled circles) as a function of the applied gate voltage.

$$n = -\frac{C^3}{e\epsilon_0\epsilon_r A^2} \frac{1}{dC/dV} \quad (4)$$

In Fig. 7 a comparison between the simulated and the measured data is shown. For the calculations a dielectric constant of 9.7 for GaN was assumed [2]. A good agreement between the measurement points and the simulation curve by PSM is observed. Assuming a width of 10 nm for the two dimensional electron channel at the hetero-interface the sheet carrier concentration is calculated to $9 \times 10^{12} \text{ cm}^{-2}$.

The form of the C-V curve in section between -3.5 V and -5 V depends on the donor concentration in the GaN buffer layer.

In summary, the following parameters are obtained from the measured curve by comparison with the simulations. A donor concentration of $9 \times 10^{16} \text{ cm}^{-3}$ in the GaN bulk and about $1.8 \times 10^{18} \text{ cm}^{-3}$ in the $\text{Al}_{0.39}\text{Ga}_{0.61}\text{N}$ layer is obtained. An electron concentration for the accumulation layer at the heterostructure interface of $9 \times 10^{12} \text{ cm}^{-2}$ is estimated.

5 Conclusions Cubic AlGaIn/GaN hetero structures were fabricated by PAMBE on freestanding 3C-SiC. A clear evidence for an electron accumulation layer from C-V measurements of SiO_2 -AlGaIn/GaN MOSH structures is obtained. Using a self consistent Poisson-Schrödinger model C-V-curves of these structures were simulated and a good agreement between theory and experimental results is reached. Conduction channel charge carrier concentration at the heterointerface of $9 \times 10^{12} \text{ cm}^{-2}$ is estimated.

Acknowledgements The authors acknowledge financial support by „Deutsche Forschungsgemeinschaft“, project No. As 107/4-1. We also thank H. Nagasawa and M. Abe, HOYA Corporation, SiC Development Center, 1-17-16 Tanashioda, Sagami-hara, Kanagawa 229-1125, Japan for supply of 3C-SiC substrates.

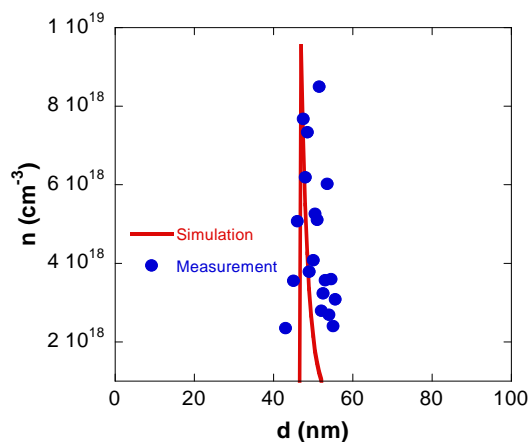


Figure 7 Electron concentration n as a function of the distance d from the sample surface. Comparison between measured and simulated data.

References

- [1] J. Schörmann, S. Potthast, D. J. As, and K. Lischka, Appl. Phys. Lett. **89**, 131910 (2006).
- [2] D. J. As, in: Optoelectronic Properties of Semiconductors and Superlattices, series editor M. O. Manasreh (Taylor and Francis Books, Inc., New York, 2003), Vol. 19, chap. 9 pp. 323-450.
- [3] J. Schörmann, S. Potthast, D. J. As, and K. Lischka, Appl. Phys. Lett. **90**, 041918 (2007).
- [4] I. H. Tan, G. Snider, and E. L. Hu, J. Appl. Phys. **68**, 4071 (1990).
- [5] W. C. Johnson et al., IEEE Trans. Electron Dev. **18**(10), 965 (1971).