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Electrical properties of MBE grown Si_3N_4–cubic GaN MIS structures

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In this work we report on the electrical characterization of non-polar cubic GaN metal-insulator-semiconductor (MIS) structures. Si_3N_4 layers were deposited *in-situ* on top of cubic GaN grown on 3C-SiC (001) substrates. The electric characteristics of the MIS structures are measured by capacitance and admittance spectroscopy techniques. From the hysteresis in the capacitance-voltage curves and the peak height of the conductance G_p–ω frequency curves the interface state densities are calculated. We find interface traps about 0.3 eV below the conduction band. The density of these traps is D_{it} = 2.5x10^{11} cm^{-2}eV^{-1}. This is one order of magnitude lower than in MIS structures with a Si_3N_4 insulator produced by plasma enhanced vapour deposition and two orders of magnitude lower than in MIS structures on c-GaN with SiO_2 as insulator.

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1 Introduction Recently, the first hetero junction field effect transistor (HFET) with normally off characteristics based on cubic AlGaN/GaN heterostructure [1] was realized. However, the critical issue in the operation of this device was its high gate leakage current, which is undesirable for high power and low noise applications and severely reduces the device performance. Therefore, the use of metal/insulator layers instead of a Schottky gate, leading to the metal-insulator-semiconductor heterojunction field effect transistors (MIS-HFET), is proposed for improved device characteristics [2,3].

For III-V compounds like GaN or GaAs gate insulators usually used are SiO_2 and Si_3N_4. These insulators are mainly deposited by plasma enhanced chemical vapor deposition (PECVD) [4,5]. However, during transport to the PECVD chamber the c-GaN surface is exposed to atmosphere, which may lead to the formation of additional defect states. A sufficient high quality of the interface between the insulator and nitride epilayer, however is one critical issue of any MIS structure. Growing Si_3N_4 *in-situ* - directly in the MBE chamber after the growth of c-GaN - may prevent the formation of such defect states.

In this work we report on capacity vs. voltage (CV) and conductance vs. frequency ($G_p/\omega-\omega$) characteristics [6] of cubic GaN MIS structures with *in-situ* MBE-grown Si_3N_4. The results are compared with Si_3N_4 and SiO_2 layers produced ex-situ by a plasma enhanced chemical vapor deposition (PECVD) process and it is shown that *in-situ* grown Si_3N_4 has a severely reduced interface trap density.

2 Experimental The optimum conditions for the growth of cubic GaN are mainly determined by two parameters, namely the surface stoichiometry and the substrate temperature [7]. Both parameters are interrelated therefore an in-situ control of both is necessary. This is achieved by monitoring the growth process by reflection high energy electron diffraction (RHEED). The 600 nm thick cubic GaN buffer layers were grown at 720 °C on free standing, highly n-doped 3C-SiC (001) substrates, the growth rate was 150 nm/h. In order to minimize hexagonal inclusions in our layers and to obtain an optimum interface roughness a coverage of 1 monolayer Ga was established during growth [8].

In our experiments two kinds of sample structures were investigated. In the first series the 600 nm thick c-GaN layers were taken out from the MBE chamber and Si_3N_4 layers were deposited by plasma enhanced chemical vapour deposition (PECVD) at a substrate temperature of 300 °C. The pressure during the deposition was 1.33 mbar the deposition rate was 16 nm/min. The deposited insulator thickness was estimated from the saturation region of the CV curves assuming a dielectric constant of 7.5 for Si_3N_4 [8]. In the second series Si_3N_4 layers were deposited *in-situ* in the MBE chamber directly after the growth of the c-GaN

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buffer using the nitrogen plasma source and the silicon thermal evaporation source. The substrate temperature for the deposition of Si_3N_4 layers was 300 °C. The growth rate of about 13 nm/h of the MBE deposited Si_3N_4 was estimated from CV characteristics. The background pressure during growth was $7x10^{-6}$ mbar and the atomic fluxes of nitrogen and silicon were $2x10^{14}$ $cm^{-2}s^{-1}$ and $1.8x10^{15}$ $cm^{-2}s^{-1}$, respectively. Using standard lithography circular contact structures with a diameter of 100 µm were placed on top of the insulating layer. Metal gate contacts were thermally evaporated consisting of 15 nm Ni and 50 nm Au. The ohmic back contacts were realized by soldering the highly conductive 3C-SiC on Cu plates with In. Current-voltage measurements were done with an Agilent Precision Semiconductor Parameter Analyzer 4156C. The MIS capacitors were characterized by means of CV and *G*-*ω* measurements using an Agilent Precision E4980A LCR meter. The dc bias was varied from deep depletion to accumulation and back to deep depletion. An ac-amplitude of 50 mV was used and the measurements were performed under light-tight and electrically shielded environment. The influence of the hysteresis effect was observed by CV techniques. Interface trap density values D_{it} have been extracted by admittance spectroscopy.

3 Results and discussion Typical CV curves of cubic GaN MIS structures measured at 1 MHz, are shown in Fig. 1. The capacity of MBE grown (red curve) and PECVD produced (black curve) MIS structures are depicted. To illustrate the effect of mobile charges incorporated into the insulator the bias voltage was varied from -20 V to +20 V and a hysteresis effect is depicted.

The accumulation capacitance was used to determine the equivalent insulator thickness (EIT). The EIT of the PECVD produced Si_3N_4 is 93 nm and 102 nm of the MBE produced silicon nitride (Fig. 1). For negative bias voltages no inversion capacitance is observed. With decreasing voltage the capacitance drops and does not saturate. This deep depletion feature is typical for wide band gap semiconductor MIS structures, because the generation rate of the minority carriers (holes) is extremely low at room temperature. Due to the large time constant resulting from an extremely low generation rate of holes the electron quasi-Fermi level will remain unchanged.

However, for the bias sweep back to depletion the CV curve of the MIS structure produced in the MBE chamber shows a shift of about -5 V. In contrast the CV curve of PECVD produced MIS structure shifts about 11 V. This larger shift indicates a higher density of mobile charges. We further suppose that these carriers have the opposite charge of those observed with MBE produced Si_3N_4 MIS structures.

A very sensitive technique for characterizing insulator-semiconductor interface properties relies on characterizing the interface trap conductance by directly measuring the energy loss during capture and emission of the majority carriers (electrons) between conduction band and interface trap levels under applied ac signal [10,11].

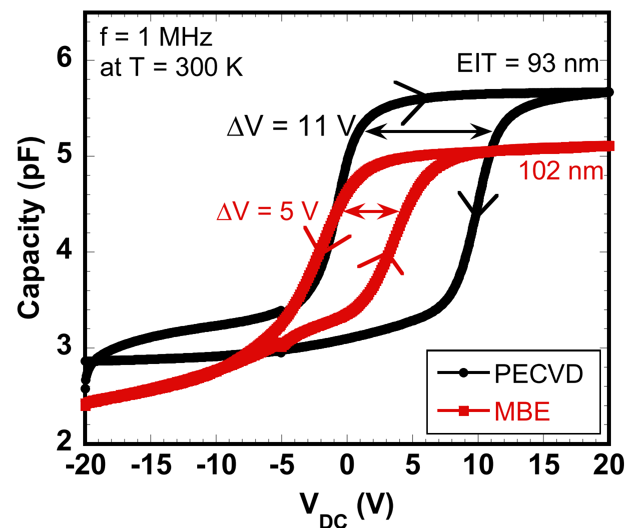

Figure 1 CV characteristics of PECVD (black curve) and MBE (red curve) produced Si_3N_4 MIS structures.

After series and insulator capacitance correction, the remaining parallel conductance G_p value only includes interface trap information. The equivalent parallel conductance G_p divided by ω is given by

$$\frac{G_p}{\omega} = \frac{C_{it}\omega\tau_{it}}{1+\omega^2\tau_{it}^2} \tag{1}$$

where ω=2π*f* and τ_{it} is the interface trap lifetime [9]. At a given bias voltage, the plot of G_p/ω versus ω goes through a maximum when $\omega\tau_{it}$=1, and thus gives τ_{it}. The value of G_p/ω at the maximum is $C_{it}/2$, where C_{it} is the capacity associated to the interface traps. Once C_{it} is known, the interface trap density is obtained by using the relationship:

$$D_{it} = \frac{C_{it}}{q_{el}A} \tag{2}$$

where *A* is the metal contact area and q_{el} the single electron charge.

Figure 2a shows G_p/ω versus frequency curves measured at different bias voltages with a PECVD produced structure. The peak shifts to higher frequencies at positive voltages between 5 V and 8 V indicating a continuous distribution of interface states within the band gap. Simultaneously the peak intensity increases.

In Fig. 2b the G_p/ω versus ω curves of the MBE produced sample are shown. Nearly no shift of the maximum is observed in this sample. The interface trap density which is proportional to the peak height is one order of magnitude lower than for the PECVD sample.

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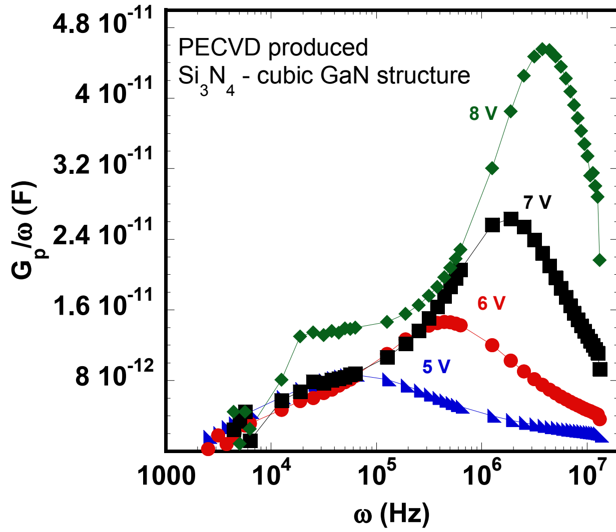

Figure 2a G_p/ω versus ω curves for the PECVD sample.

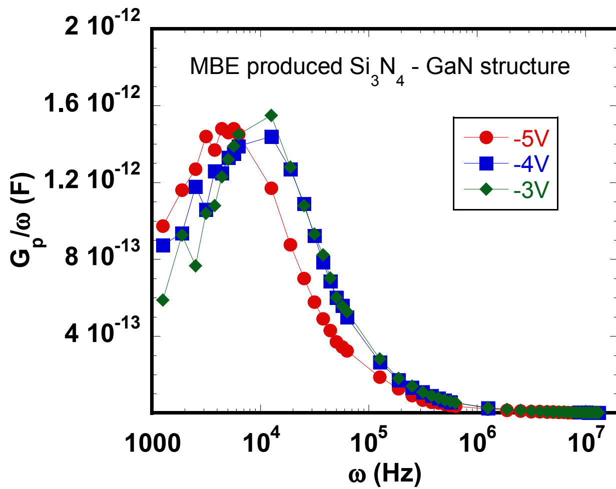

Figure 2b G_p/ω versus ω curves for the MBE sample.

The interface trap lifetime τ_{it} is given by the Shockley-Read-Hall model [12]:

$$\tau_{it}(E_{it}) = \frac{1}{\sigma_{0n} v_{th} N_C} \exp\left(\frac{E_C - E_{it}}{k_B T}\right) \quad (3)$$

where N_C is the effective density of states in the conduction band, v_{th} the thermal velocity of electrons, σ_{0n} the capture cross section of the trap, E_C the conduction band edge, k_B the Boltzmann constant and T the temperature.

The frequency ω_{max} at the maximum of G_p/ω gives $\tau_{it}=1/\omega_{max}$ and correlates ω_{max} to a corresponding trap energy level E_{it} below the conduction band edge. The thermal velocity and density of states are well known and well defined for a specific semiconductor, whereas the capture cross section of the traps depends strongly on the nature of the trap. The capture cross section can take values varying

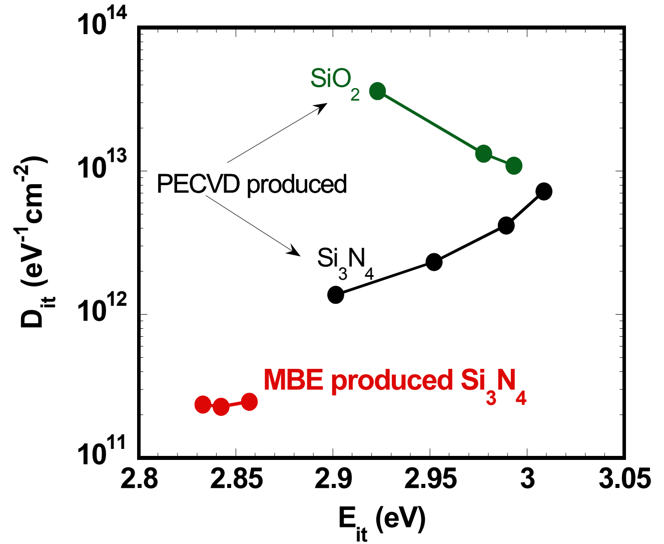

Figure 3 Interface state density D_{it} vs. energy E_{it} within the band gap of c-GaN.

from 10^{-12} cm² to 10^{-20} cm². Since up to now this value is not known for cubic GaN we assume in analogy to MBE-grown GaAs a capture cross section of 10^{-15} cm² [13] to convert τ_{it} into trap level energies.

In Fig. 3 we plot the obtained density of states of interface states D_{it} versus energy of the trap level in the gap of c-GaN. An increase of $D_{it}(E_{it})$ with increasing energy is observed in structures with Si_3N_4 produced by PECVD. This indicates a distribution of interface defect levels about 0.3 eV below the conduction band with a maximum trap density of about 2×10^{12} cm^{-2}eV^{-1}. In structures with Si_3N_4 produced by plasma assisted MBE the trap states seem to have less energy spread. We find a maximum trap density of 2.5×10^{11} cm^{-2}eV^{-1} about 0.4 eV below the conduction band edge. Thus growth of Si_3N_4 under high vacuum conditions in the MBE chamber directly after the growth of cubic GaN reduces the interface trap density by more than one order of magnitude. Since the interface is not in contact with the atmosphere the incorporation of impurities causing traps or mobile charges in the Si_3N_4 layer is significantly reduced. For comparison we also include in Fig. 3 the energy distribution of interface traps of SiO_2/c-GaN MIS structures [14]. The interface trap density in these structures is in the range of 10^{13} cm^{-2}eV^{-1}, two orders of magnitude higher than in Si_3N_4/c-GaN layers produced by MBE method.

4 Conclusions We have fabricated metal-insulator-semiconductor structures with non-polar cubic GaN deposited on highly conductive 3C-SiC (001) substrates. The trap energy and trap densities in MIS structures produced *in-situ* by molecular beam epitaxy and *ex-situ* by plasma enhanced chemical vapor deposition are compared. The MBE produced structure shows a reduced hysteresis effect in the CV curve indicating a lower density of mobile

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charges. By admittance spectroscopy interface traps were detected between 0.2 eV and 0.4 eV below the conduction band edge. A minimum of interface defect density of D_{it} = 2.5×10^{11} $cm^{-2}eV^{-1}$ was estimated for such Si_3N_4/c-GaN structures. This value is one order of magnitude lower than that in the PECVD produced Si_3N_4 structure and two orders of magnitude lower than that measured with SiO_2 insulator layers. Our results demonstrate that MBE produced *in-situ* Si_3N_4 layers have a great potential as gate dielectrics in MIS structures on c-GaN.

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